

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
15 August 2002 (15.08.2002)

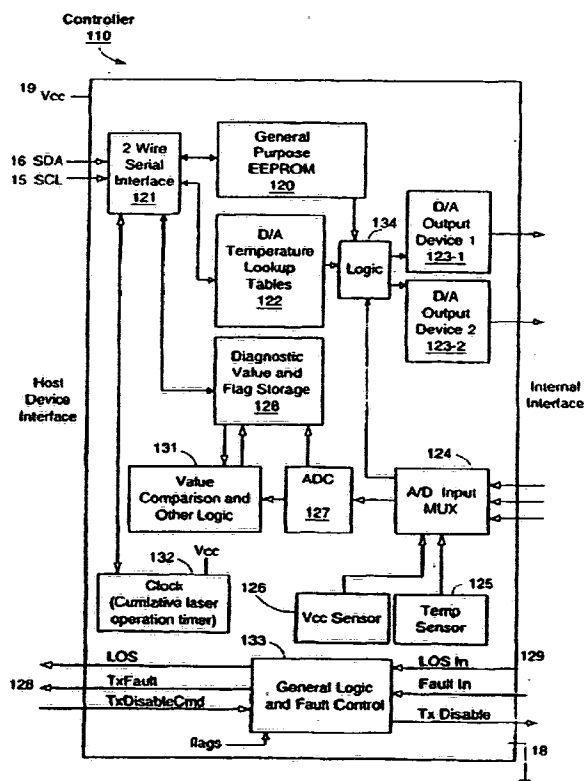
PCT

(10) International Publication Number
WO 02/063800 A1

- (51) International Patent Classification: H04B 10/00 (74) Agents: WILLIAMS, Gary, S. et al.: Pennie & Edmonds LLP, 1155 Avenue of the Americas, New York, NY 10036 (US).
- (21) International Application Number: PCT/US02/03226
- (22) International Filing Date: 4 February 2002 (04.02.2002) (81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data: 09/777,917 5 February 2001 (05.02.2001) US
- (71) Applicant: FINISAR CORPORATION [US/US]; 1308 Moffett Park Drive, Sunnyvale, CA 94089-1133 (US).
- (72) Inventors: ARONSON, Lewis, B.; 794 Manor Way, Los Altos, CA 94024 (US). HOSKING, Stephen, G.; 320 Swift Street, Santa Cruz, CA 95060 (US).
- (84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: INTEGRATED MEMORY CONTROLLER CIRCUIT FOR FIBER OPTICS TRANSCEIVER



(57) Abstract: A controller (110) for controlling a transceiver having a laser transmitter and a photodiode receiver. The controller includes memory (120, 122, 128) for storing information related to the transceiver, and analog to digital conversion circuitry (127) for receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory. Comparison logic (131) compares one or more of these digital values with limit values, generates flag values based on the comparisons, and stores the flag values in predefined locations within the memory. Control circuitry (123-1, 123-2) in the controller controls the operation of the laser transmitter in accordance with one or more values stored in the memory. A serial interface (121) is provided to enable a host device to read from and write to locations within the memory. Excluding a small number of binary input and output signals, all control and monitoring functions of the transceiver are mapped to unique memory mapped locations within the controller. A plurality of the control functions and a plurality of the monitoring functions of the controller are exercised by a host computer by accessing corresponding memory mapped locations within the controller.

BEST AVAILABLE COPY

INTEGRATED MEMORY MAPPED CONTROLLER CIRCUIT FOR FIBER OPTICS TRANSCEIVER

The present invention relates generally to the field of fiber optic transceivers and particularly to circuits used within the transceivers to accomplish control, setup, monitoring, and identification operations.

5 BACKGROUND OF INVENTION

The two most basic electronic circuits within a fiber optic transceiver are the laser driver circuit, which accepts high speed digital data and electrically drives an LED or laser diode to create equivalent optical pulses, and the receiver circuit which takes relatively small signals from an optical detector and amplifies and limits them to
10 create a uniform amplitude digital electronic output. In addition to, and sometimes in conjunction with these basic functions, there are a number of other tasks that must be handled by the transceiver circuitry as well as a number of tasks that may optionally be handled by the transceiver circuit to improve its functionality. These tasks include, but are not necessarily limited to, the following:

- 15 • Setup functions. These generally relate to the required adjustments made on a part-to-part basis in the factory to allow for variations in component characteristics such as laser diode threshold current.
- Identification. This refers to general purpose memory, typically EEPROM (electrically erasable and programmable read only memory) or other nonvolatile
20 memory. The memory is preferably accessible using a serial communication standard, that is used to store various information identifying the transceiver type, capability, serial number, and compatibility with various standards. While not standard, it would be desirable to further store in this memory additional information, such as sub-component revisions and factory test data.

implemented using discrete circuitry, for example using a general purpose EEPROM for identification purposes, by inclusion of some functions within the laser driver or receiver circuitry (for example some degree of temperature compensation in a laser driver circuit) or with the use of a commercial micro-controller integrated circuit.

- 5 However, to date there have not been any transceivers that provide a uniform device architecture that will support all of these functions, as well as additional functions not listed here, in a cost effective manner.

It is the purpose of the present invention to provide a general and flexible integrated circuit that accomplishes all (or any subset) of the above functionality using
10 a straightforward memory mapped architecture and a simple serial communication mechanism.

Fig. 1 shows a schematic representation of the essential features of a typical prior-art fiber optic transceiver. The main circuit 1 contains at a minimum transmit and receiver circuit paths and power 19 and ground connections 18. The receiver
15 circuit typically consists of a Receiver Optical Subassembly (ROSA) 2 which contains a mechanical fiber receptacle as well as a photodiode and pre-amplifier (preamp) circuit. The ROSA is in turn connected to a post-amplifier (postamp) integrated circuit 4, the function of which is to generate a fixed output swing digital signal which is connected to outside circuitry via the RX+ and RX- pins 17. The postamp circuit
20 also often provides a digital output signal known as Signal Detect or Loss of Signal indicating the presence or absence of suitably strong optical input. The Signal Detect output is provided as an output on pin 18. The transmit circuit will typically consist of a Transmitter Optical Subassembly (TOSA), 3 and a laser driver integrated circuit 5. The TOSA contains a mechanical fiber receptacle as well as a laser diode or LED.
25 The laser driver circuit will typically provide AC drive and DC bias current to the laser. The signal inputs for the AC driver are obtained from the TX+ and TX- pins 12. Typically, the laser driver circuitry will require individual factory setup of certain parameters such as the bias current (or output power) level and AC modulation drive to the laser. Typically this is accomplished by adjusting variable resistors or placing
30 factory selected resistors 7, 9 (i.e., having factory selected resistance values). Additionally, temperature compensation of the bias current and modulation is often

one or more of these digital values with limit values, generates flag values based on the comparisons, and stores the flag values in predefined locations within the memory. Control circuitry in the controller controls the operation of the laser transmitter in accordance with one or more values stored in the memory. A serial interface is
5 provided to enable a host device to read from and write to locations within the memory. A plurality of the control functions and a plurality of the monitoring functions of the controller are exercised by a host computer by accessing corresponding memory mapped locations within the controller.

In some embodiments the controller further includes a cumulative clock for
10 generating a time value corresponding to cumulative operation time of the transceiver, wherein the generated time value is readable via the serial interface.

In some embodiments the controller further includes a power supply voltage sensor that generates a power level signal corresponding to a power supply voltage level of the transceiver. In these embodiments the analog to digital conversion
15 circuitry is configured to convert the power level signal into a digital power level value and to store the digital power level value in a predefined power level location within the memory. Further, the comparison logic of the controller may optionally include logic for comparing the digital power level value with a power (i.e., voltage) level limit value, generating a flag value based on the comparison of the digital power
20 level signal with the power level limit value, and storing a power level flag value in a predefined power level flag location within the memory. It is noted that the power supply voltage sensor measures the transceiver voltage supply level, which is distinct from the power level of the received optical signal.

In some embodiments the controller further includes a temperature sensor that
25 generates a temperature signal corresponding to a temperature of the transceiver. In these embodiments the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory. Further, the comparison logic of the controller may optionally include logic for comparing the
30 digital temperature value with a temperature limit value, generating a flag value based on the comparison of the digital temperature signal with the temperature limit value,

invention. It is noted that Memory Map Tables 1, 2, 3 and 4, in addition to showing a memory map of values and control features described in this document, also show a number of parameters and control mechanisms that are outside the scope of this document and thus are not part of the present invention.

5 The interface 121 is coupled to host device interface input/output lines, typically clock (SCL) and data (SDA) lines, 15 and 16. In the preferred embodiment, the serial interface 121 operates in accordance with the two wire serial interface standard that is also used in the GBIC and SFP standards, however other serial interfaces could equally well be used in alternate embodiments. The two wire serial
10 interface 121 is used for all setup and querying of the controller IC 110, and enables access to the optoelectronic transceiver's control circuitry as a memory mapped device. That is, tables and parameters are set up by writing values to predefined memory locations of one or more nonvolatile memory devices 120, 122, 128 (e.g., EEPROM devices) in the controller, whereas diagnostic and other output and status
15 values are output by reading predetermined memory locations of the same nonvolatile memory devices 120, 121, 122. This technique is consistent with currently defined serial ID functionality of many transceivers where a two wire serial interface is used to read out identification and capability data stored in EEPROM.

It is noted here that some of the memory locations in the memory devices 120,
20 122, 128 are dual ported, or even triple ported in some instances. That is, while these memory mapped locations can be read and in some cases written via the serial interface 121, they are also directly accessed by other circuitry in the controller 110. For instance, certain "margin" values stored in memory 120 are read and used directly by logic 134 to adjust (i.e., scale upwards or downwards) drive level signals
25 being sent to the D/A output devices 123. Similarly, there are flags stored memory 128 that are (A) written by logic circuit 131, and (B) read directly by logic circuit 133. An example of a memory mapped location not in memory devices but that is effectively dual ported is the output or result register of clock 132. In this case the accumulated time value in the register is readable via the serial interface 121, but is
30 written by circuitry in the clock circuit 132.

implemented in the controller 110 through the use of temperature lookup tables 122 that are used to assign values to the control outputs as a function of the temperature measured by a temperature sensor 125 within the controller IC 110. In alternate embodiments, the controller 110 may use D/A converters with voltage source outputs
5 or may even replace one or more of the D/A converters 123 with digital potentiometers to control the characteristics of the laser driver 105. It should also be noted that while Fig. 2 refers to a system where the laser driver 105 is specifically designed to accept inputs from the controller 110, it is possible to use the controller IC 110 with many other laser driver ICs to control their output characteristics.

10 In addition to temperature dependent analog output controls, the controller IC may be equipped with a multiplicity of temperature independent (one memory set value) analog outputs. These temperature independent outputs serve numerous functions, but one particularly interesting application is as a fine adjustment to other settings of the laser driver 105 or postamp 104 in order to compensate for process
15 induced variations in the characteristics of those devices. One example of this might be the output swing of the receiver postamp 104. Normally such a parameter would be fixed at design time to a desired value through the use of a set resistor. It often turns out, however, that normal process variations associated with the fabrication of the postamp integrated circuit 104 induce undesirable variations in the resulting
20 output swing with a fixed set resistor. Using the present invention, an analog output of the controller IC 110, produced by an additional D/A converter 123, is used to adjust or compensate the output swing setting at manufacturing setup time on a part-by-part basis.

In addition to the connection from the controller to the laser driver 105, Fig. 2
25 shows a number of connections from the laser driver 105 to the controller IC 110, as well as similar connections from the ROSA 106 and Postamp 104 to the controller IC 110. These are analog monitoring connections that the controller IC 110 uses to provide diagnostic feedback to the host device via memory mapped locations in the controller IC. The controller IC 110 in the preferred embodiment has a multiplicity of
30 analog inputs. The analog input signals indicate operating conditions of the transceiver and/or receiver circuitry. These analog signals are scanned by a

The limit flags are also sometimes call alarm and warning flags. The host device (or end user) can monitor these flags to determine whether conditions exist that are likely to have caused a transceiver link to fail (alarm flags) or whether conditions exist which predict that a failure is likely to occur soon. Examples of such conditions might be a laser bias current which has fallen to zero, which is indicative of an immediate failure of the transmitter output, or a laser bias current in a constant power mode which exceeds its nominal value by more than 50%, which is an indication of a laser end-of-life condition. Thus, the automatically generated limit flags are useful because they provide a simple pass-fail decision on the transceiver functionality based on internally stored limit values.

In a preferred embodiment, fault control and logic circuit 133 logically OR's the alarm and warning flags, along with the internal LOS (loss of signal) input and Fault Input signals, to produce a binary Transceiver fault (TxFault) signal that is coupled to the host interface, and thus made available to the host device. The host device can be programmed to monitor the TxFault signal, and to respond to an assertion of the TxFault signal by automatically reading all the alarm and warning flags in the transceiver, as well as the corresponding monitored signals, so as to determine the cause of the alarm or warning.

The fault control and logic circuit 133 furthermore conveys a loss of signal (LOS) signal received from the receiver circuit (ROSA, Fig. 2) to the host interface.

Another function of the fault control and logic circuit 133 is to disable the operation of the transmitter (TOSA, Fig. 2) when needed to ensure eye safety. There is a standards defined interaction between the state of the laser driver and the Tx Disable output, which is implemented by the fault control and logic circuit 133. When the logic circuit 133 detects a problem that might result in an eye safety hazard, the laser driver is disabled by activating the Tx Disable signal of the controller. The host device can reset this condition by sending a command signal on the TxDisableCmd line of the host interface.

Yet another function of the fault control and logic circuit 133 is to determine the polarity of its input and output signals in accordance with a set of configuration flags stored in memory 128. For instance, the Loss of Signal (LOS) output of circuit

TABLE 1
MEMORY MAP FOR TRANSCEIVER CONTROLLER

Memory Location (Array 0)	Name of Location	Function
00h - 5Fh	IEEE Data	This memory block is used to store required GBIC data
60h	Temperature MSB	This byte contains the MSB of the 15-bit 2's complement temperature output from the temperature sensor.
61h	Temperature LSB	This byte contains the LSB of the 15-bit 2's complement temperature output from the temperature sensor. (LSB is 0b).
62h - 63h	V _{cc} Value	These bytes contain the MSB (62h) and the LSB (63h) of the measured V _{cc} (15-bit number, with a 0b LSbit)
64h - 65h	B _m Value	These bytes contain the MSB (64h) and the LSB (65h) of the measured B _m (laser bias current) (15-bit number, with a 0b LSbit)
66h - 67h	P _m Value	These bytes contain the MSB (66h) and the LSB (67h) of the measured P _m (transmitted laser power) (15-bit number, with a 0b LSbit)
68h - 69h	R _m Value	These bytes contain the MSB (68h) and the LSB (69h) of the measured R _m (received power) (15-bit number, with a 0b LSbit)
6Ah - 6Dh	Reserved	Reserved
6Eh	IO States	This byte shows the logical value of the I/O pins
6Fh	A/D Updated	Allows the user to verify if an update from the A/D has occurred to the 5 values: temperature, V _{cc} , B _m , P _m and R _m . The user writes the byte to 00h. Once a conversion is complete for a give value, its bit will change to '1'.
70h - 73h	Alarm Flags	These bits reflect the state of the alarms as a conversion updates. High alarm bits are '1' if converted value is greater than corresponding high limit. Low alarm bits are '1' if converted value is less than corresponding low limit. Otherwise, bits are 0b.
74h - 77h	Warning Flags	These bits reflect the state of the warnings as a conversion updates. High warning bits are '1' if converted value is greater than corresponding high limit. Low warning bits are '1' if converted value is less than corresponding low limit. Otherwise, bits are 0b.
78h - 7Ah	Reserved	Reserved

	Memory Location (Array 3)	Name of Location	Function of Location
5	84h - 85h 8Ch - 8Dh 94h - 95h 9Ch - 9Dh A4h - A5h	Temp High Warning V _{cc} High Warning B _{in} High Warning P _{in} High Warning R _{in} High Warning	The value written to this location serves as the high warning limit. Data format is the same as the corresponding value (temperature, V _{cc} , B _{in} , P _{in} , R _{in}).
10	86h - 87h 8Eh - 8Fh 96h - 97h 9Eh - 9Fh A6h - A7h	Temperature Low Warning V _{cc} Low Warning B _{in} Low Warning P _{in} Low Warning R _{in} Low Warning	The value written to this location serves as the low warning limit. Data format is the same as the corresponding value (temperature, V _{cc} , B _{in} , P _{in} , R _{in}).
15	A8h - AFh, C5h B0h - B7h, C6h B8h - BFh, C7h	D _{out} control 0-8 F _{out} control 0-8 L _{out} control 0-8	Individual bit locations are defined in Table 4.
	C0h	Reserved	Reserved
20	C1h	Prescale	Selects MCLK divisor for X-delay CLKS.
	C2h C3h C4h	D _{out} Delay F _{out} Delay L _{out} Delay	Selects number of prescale clocks
25	C8h - C9h CAh - CBh CCh - CDh CEh - CFh	V _{cc} - A/D Scale B _{in} - A/D Scale P _{in} - A/D Scale R _{in} - A/D Scale	16 bits of gain adjustment for corresponding A/D conversion values.
	D0h	Chip Address	Selects chip address when external pin ASEL is low.
	D1h	Margin #2	Finisar Selective Percentage (FSP) for D/A #2
	D2h	Margin #1	Finisar Selective Percentage (FSP) for D/A #1
30	D3h - D6h	PW1 Byte 3 (D3h) MSB PW1 Byte 2 (D4h) PW1 Byte 1 (D5h) PW1 Byte 0 (D6h) LSB	The four bytes are used for password 1 entry. The entered password will determine the Finisar customer's read/write privileges.
35	D7h	D/A Control	This byte determines if the D/A outputs source or sink current, and it allows for the outputs to be scaled.
	D8h - DFh	B _{in} Fast Trip	These bytes define the fast trip comparison over temperature.
	E0h - E3h	P _{in} Fast Trip	These bytes define the fast trip comparison over temperature.

TABLE 2 - DETAIL MEMORY DESCRIPTIONS - A/D VALUES AND STATUS BITS

Byte	Bit	Name	Description	
Converted analog values. Calibrated 16 bit data.				
5	96 (60h)	Temperature MSB	Signed 2's complement integer temperature (-40 to +125C) Based on internal temperature measurement	
	97	Temperature LSB	Fractional part of temperature (count/256)	
	98	V _{cc} MSB	Internally measured supply voltage in transceiver. Actual voltage is full 16 bit value * 100 uVolt.	
10	99	V _{cc} LSB	(Yields range of 0 - 6.55V)	
	100	TX Bias MSB	Measured TX Bias Current in mA Bias current is full 16 bit value *(1/256) mA.	
	101	TX Bias LSB	(Full range of 0 - 256 mA possible with 4 uA resolution)	
15	102	TX Power MSB	Measured TX output power in mW. Output is full 16 bit value *(1/2048) mW.	
	103	TX Power LSB	Full range of 0 - 32 mW possible with 0.5 μW resolution, or -33 to +15 dBm)	
20	104	RX Power MSB	Measured RX input power in mW RX power is full 16 bit value *(1/16384) mW.	
	105	RX Power LSB	(Full range of 0 - 4 mW possible with 0.06 μW resolution, or -42 to +6 dBm)	
	106	Reserved MSB	Reserved for 1 st future definition of digitized analog input	
25	107	Reserved LSB	Reserved for 1 st future definition of digitized analog input	
	108	Reserved MSB	Reserved for 2 nd future definition of digitized analog input	
30	109	Reserved LSB	Reserved for 2 nd future definition of digitized analog input	
General Status Bits				
35	110	7	TX Disable	Digital state of the TX Disable Input Pin
	110	6	Reserved	
	110	5	Reserved	
	110	4	Rate Select	Digital state of the SFP Rate Select Input Pin
	110	3	Reserved	
	110	2	TX Fault	Digital state of the TX Fault Output Pin
	110	1	LOS	Digital state of the LOS Output Pin
40	110	0	Power-On-Logic	Indicates transceiver has achieved power up and data valid
	111	7	Temp A/D Valid	Indicates A/D value in Bytes 96/97 is valid
	111	6	V _{cc} A/D Valid	Indicates A/D value in Bytes 98/99 is valid

TABLE 3 - DETAIL MEMORY DESCRIPTIONS - ALARM AND WARNING FLAG BITS

Byte	Bit	Name	Description	
Alarm and Warning Flag Bits				
5	112	7	Temp High Alarm	Set when internal temperature exceeds high alarm level.
	112	6	Temp Low Alarm	Set when internal temperature is below low alarm level.
10	112	5	V _{cc} High Alarm	Set when internal supply voltage exceeds high alarm level.
	112	4	V _{cc} Low Alarm	Set when internal supply voltage is below low alarm level.
	112	3	TX Bias High Alarm	Set when TX Bias current exceeds high alarm level.
15	112	2	TX Bias Low Alarm	Set when TX Bias current is below low alarm level.
	112	1	TX Power High Alarm	Set when TX output power exceeds high alarm level.
20	112	0	TX Power Low Alarm	Set when TX output power is below low alarm level.
	113	7	RX Power High Alarm	Set when Received Power exceeds high alarm level.
	113	6	RX Power Low Alarm	Set when Received Power is below low alarm level.
25	113	5-0	Reserved Alarm	
	114	All	Reserved	
	115	All	Reserved	
	116	7	Temp High Warning	Set when internal temperature exceeds high warning level.
30	116	6	Temp Low Warning	Set when internal temperature is below low warning level.
	116	5	V _{cc} High Warning	Set when internal supply voltage exceeds high warning level.
35	116	4	V _{cc} Low Warning	Set when internal supply voltage is below low warning level.
	116	3	TX Bias High Warning	Set when TX Bias current exceeds high warning level.
	116	2	TX Bias Low Warning	Set when TX Bias current is below low warning level.
40	116	1	TX Power High Warning	Set when TX output power exceeds high warning level.
	116	0	TX Power Low Warning	Set when TX output power is below low warning level.
45	117	7	RX Power High Warning	Set when Received Power exceeds high warning level.

TABLE 4

Byte Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5 X-out cnt10	T alrm hi set	T alrm lo set	V alrm hi set	V alrm lo set	B alrm hi set	B alrm lo set	p alrm hi set	P alrm lo set
X-out cnt11	R alrm hi set	R alrm lo set	B ft hi set	P ft hi set	R ft hi set	D-in inv set	D-in set	F-in inv set
X-out cnt12	F-in set	L-in inv set	L-in set	Aux inv set	Aux set	T alrm hi hib	T alrm lo hib	V alrm hi hib
X-out cnt13	V alrm lo hib	B alrm hi hib	B alrm lo hib	P alrm hi hib	P alrm lo hib	R alrm hi hib	R alrm lo hib	B ft hi hib
X-out cnt14	P ft hi hib	R ft hi hib	D-in inv hib	D-in hib	F-in inv hib	F-in hib	L-in inv hib	L-in hib
10 X-out cnt15	Aux inv hib	Aux hib	T alrm hi clr	T alrm lo clr	V alrm hi clr	V alrm lo clr	B alrm hi clr	B alrm lo clr
X-out cnt16	P alrm hi clr	P alrm lo clr	R alrm hi clr	R alrm lo clr	B ft hi clr	P ft hi clr	R ft hi clr	D-in inv clr
X-out cnt17	D-in clr	F-in inv clr	F-in clr	L-in inv clr	L-in clr	Aux inv clr	Aux clr	EE
X-out cnt18	latch select	invert	o-ride data	o-ride select	S reset data	HI enable	LO enable	Pullup enable
15 Prescale	reserved	reserved	Reserved	reserved	B ³	B ²	B ¹	B ⁰
X-out delay	B ⁷	B ⁶	B ⁵	B ⁴	B ³	B ²	B ¹	B ⁰
chip address	b ⁷	b ⁶	b ⁵	b ⁴	b ³	b ²	b ¹	x
X-ad scale MSB	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸
20 X-ad scale LSB	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
D/A cnt1	source/sink	D/A #2 range			source/sink	D/A #1 range		
	1/0	2 ²	2 ¹	2 ⁰	1/0	2 ²	2 ¹	2 ⁰
config/O-ride	manual D/A	manual index	manual AD alarm	EE Bar	SW-POR	A/D Enable	Manual fast alarm	reserved
25 Internal State 1	D-set	D-inhibit	D-delay	D-clear	F-set	F-inhibit	F-delay	F-clear
Internal State 0	L-set	L-inhibit	L-delay	L-clear	reserved	reserved	reserved	reserved
I/O States 1	reserved	F-in	L-in	reserved	D-out	reserved	reserved	reserved
Margin #1	Reserved	Neg_Scale 2	Neg_Scale 1	Neg_Scale 0	Reserved	Pos_Scale 2	Pos_Scale 1	Pos_Scale0
30 Margin #2	Reserved	Neg_Scale 2	Neg_Scale 1	Neg_Scale 0	Reserved	Pos_Scale 2	Pos_Scale 1	Pos_Scale0

1 4. The single-chip integrated circuit of claim 3, wherein
2 the comparison logic includes logic for comparing the digital power level
3 value with a power level limit value, generating a power level flag value based on the
4 comparison of the digital power level signal with the power level limit value, and
5 storing the power level flag value in a predefined power level flag location within the
6 memory.

1 5. The single-chip integrated circuit of claim 1, further including:
2 a temperature sensor coupled to the analog to digital conversion circuitry, the
3 temperature sensor generating a temperature signal corresponding to a temperature of
4 the transceiver, wherein the analog to digital conversion circuitry is configured to
5 convert the temperature signal into a digital temperature value and to store the digital
6 temperature value in a predefined temperature location within the memory.

1 6. The single-chip integrated circuit of claim 5, wherein
2 the comparison logic includes logic for comparing the digital temperature
3 value with a temperature limit value, generating a temperature flag value based on the
4 comparison of the digital temperature signal with the temperature limit value, and
5 storing the temperature flag value in a predefined temperature flag location within the
6 memory.

1 7. The single-chip integrated circuit of claim 1, further including
2 fault handling logic, coupled to the transceiver for receiving at least one fault
3 signal from the transceiver, coupled to the memory to receive at least one flag value
4 stored in the memory, and coupled to a host interface to transmit a computed fault
5 signal, the fault handling logic including computational logic for logically combining
6 the at least one fault signal received from the transceiver and the at least one flag
7 value received from the memory to generate the computed fault signal.

1 8. A single-chip integrated circuit for controlling an optoelectronic device,
2 comprising:

5 receiving a plurality of analog signals from the laser transmitter and
6 photodiode receiver, converting the received analog signals into digital values, and
7 storing the digital values in predefined locations within the memory;
8 comparing the digital values with limit values, generating flag values based on
9 the limit values, and storing the flag values in predefined locations within the
10 memory;
11 generating control signals to control operation of the laser transmitter in
12 accordance with one or more values stored in the memory.

1 11. The method of claim 10, further including:
2 generating a time value corresponding to cumulative operation time of the
3 transceiver, wherein the generated time value is readable by the host device via the
4 memory interface.

1 12. The method of claim 10, further including:
2 converting an analog power supply voltage level signal, corresponding to a
3 voltage level of the transceiver, into a digital power level value and storing the digital
4 power level value in a predefined power level location within the memory.

1 13. The method integrated circuit of claim 12, including
2 comparing the digital power level value with a power level limit value,
3 generating a power level flag value based on the comparison of the digital power level
4 signal with the power level limit value, and storing the power level flag value in a
5 predefined power level flag location within the memory.

1 14. The method of claim 10, further including:
2 generating a temperature signal corresponding to a temperature of the
3 transceiver, converting the temperature signal into a digital temperature value and
4 storing the digital temperature value in a predefined temperature location within the
5 memory.

10 comparing the digital values with limit values, generating flag values based on
11 the limit values, and storing the flag values in predefined memory mapped locations
12 within the controller;
13 generating control signals to control operation of the laser transmitter in
14 accordance with one or more values stored in the predefined memory mapped
15 locations within the controller;
16 analog to digital conversion circuitry for receiving a plurality of analog signals
17 from the laser transmitter and photodiode receiver, converting the received analog
18 signals into digital values; and storing the digital values in predefined memory
19 mapped locations within the controller.

1 19. The method of claim 18, further including:
2 generating and storing in a register a time value corresponding to cumulative
3 operation time of the transceiver, wherein the register in which the time value is
4 accessed by the reading step as a memory mapped within the controller.

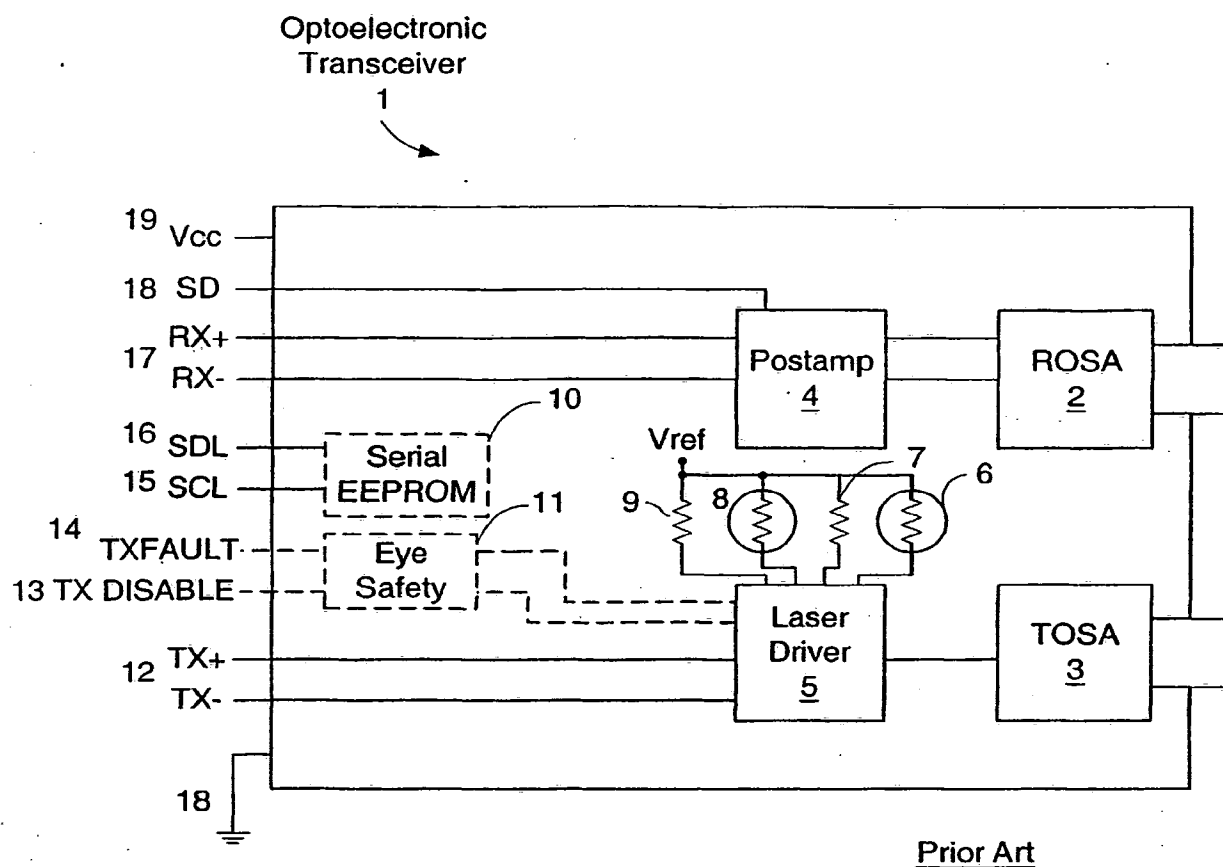


Fig. 1

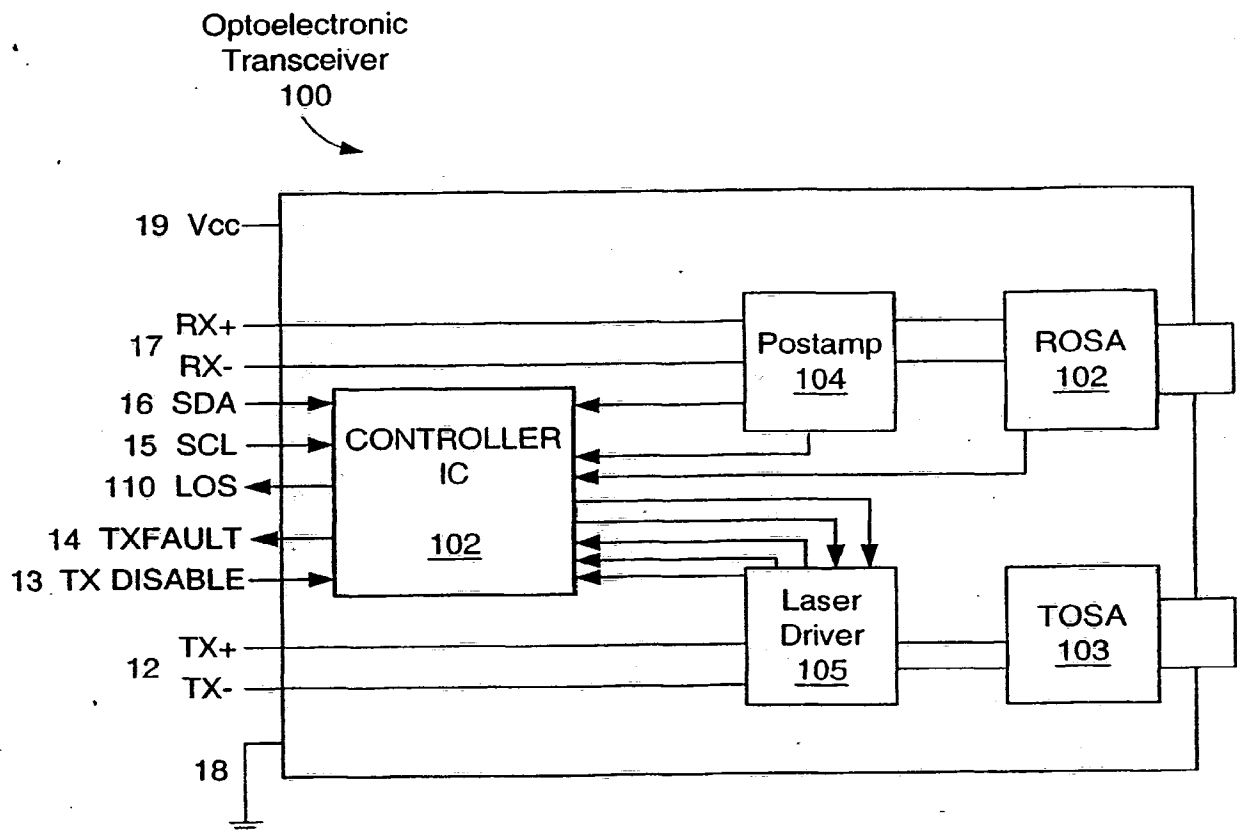
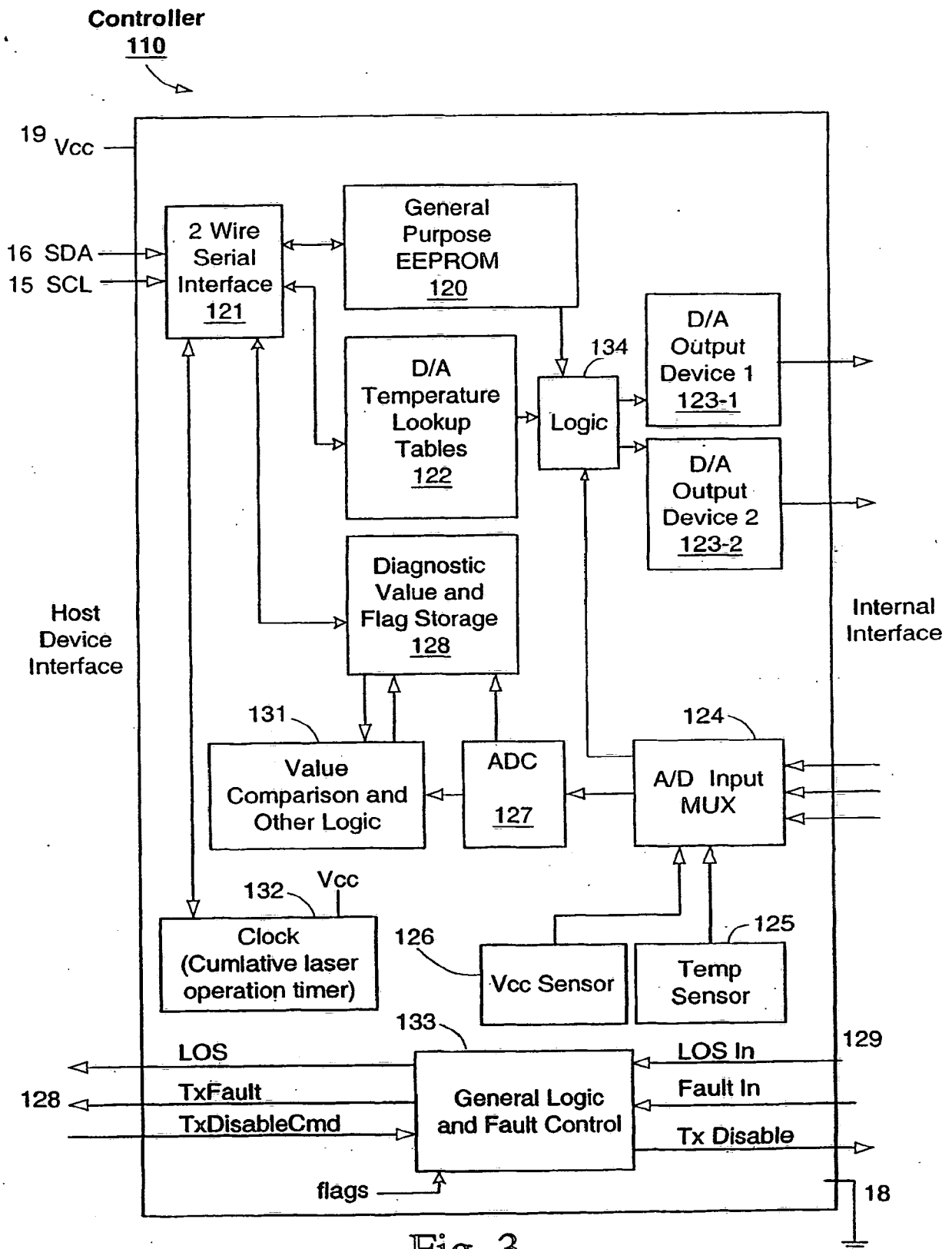


Fig. 2





P.B.5618 - Patentaan 2
2280 HV Rijswijk (ZH)
T 31 70 340 2040
TX 31651 epo nl
FAX 31 70 340 3016

Europäisches
Patentamt

Zweigstelle
in Den Haag
Forschungs-
abteilung

Eur. in
Patent Office

Branch at
The Hague
Search

Office européen
des brevets

Département à
La Haye
Division de la
recherche

Cross, Rupert Edward Blount
BOULT WADE TENNANT,
Verulam Gardens
70 Gray's Inn Road
London WC1X 8BT
GRANDE BRETAGNE

Datum/Date

05.10.04

Zeichen/Ref./Ref.

REC/P63847/000

Anmeldung Nr./Application No./Demande n°/Patent Nr./Patent No./Brevet n°.

02704344.7-2415-US0203226

Anmelder/Applicant/Demandeur/Patentinhaber/Proprietor/Titulaire

FINISAR CORPORATION

COMMUNICATION

The European Patent Office herewith transmits as an enclosure the European search report for the above-mentioned European patent application.

If applicable, copies of the documents cited in the European search report are attached.

☒ Additional set(s) of copies of the documents cited in the European search report is (are) enclosed as well.

REFUND OF THE SEARCH FEE

If applicable under Article 10 Rules relating to fees, a separate communication from the Receiving Section on the refund of the search fee will be sent later.



BEST AVAILABLE COPY



European Patent
Office

SUPPLEMENTARY
EUROPEAN SEARCH REPORT

Application Number
EP 02 70 4344

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 383 208 A (QUENIAT JEAN-FRANCOIS ET AL) 17 January 1995 (1995-01-17) * abstract * * column 1, line 35 - column 2, line 64 * * column 3, line 35 - column 8, line 67 * * figures 1,2,6 *	1-16	H01S5/068 H04B10/152 H01S5/042 H04B10/08 H04B10/28 G01M11/00
X	US 5 953 690 A (FARNES STEVEN L ET AL) 14 September 1999 (1999-09-14) * abstract * * column 1, line 50 - column 3, line 34 * * column 6, line 45 - column 7, line 22 * * column 8, line 66 - column 19, line 51 * * figures 1,2A,2B,4A,4B,5-7 *	1-16	
X	US 5 812 572 A (OLSEN DAVID D ET AL) 22 September 1998 (1998-09-22) * abstract * * column 1, line 7 - column 3, line 33 * * claims 1-16 * * figures 1,3-7,14,15 *	1-16	
X	US 5 019 769 A (LEVINSON FRANK H) 28 May 1991 (1991-05-28) * abstract * * column 2, line 66 - column 3, line 41 * * column 4, line 10 - column 7, line 37 * * column 15, lines 26-36 * * figures 3,7-12 *	1-16	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H04B H01S G01M
X	US 5 396 059 A (YEATES PAUL D) 7 March 1995 (1995-03-07) * the whole document *	1-16	
-/--			
The supplementary search report has been based on the last set of claims valid and available at the start of the search.			
Place of search Munich		Date of completion of the search 28 September 2004	Examiner Rolan Cisneros, E
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X: particularly relevant (taken alone) Y: particularly relevant (combined with another document of the same category) A: technological background O: non-written disclosure P: intermediate document</p> <p>T: Theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons a: member of the same patent family, corresponding document</p>			

2
EPO FORM 28 (to be filled in by the EPO)

BEST AVAILABLE COPY



European Patent
Office

**SUPPLEMENTARY
EUROPEAN SEARCH REPORT**

Application Number
EP 02 70 4344

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 594 748 A (JABR SALIM N) 14 January 1997 (1997-01-14) * abstract * * column 2, lines 13-54 * * column 6, line 6 - column 12, line 23 * * figures 5A,5B,7 *	1-16	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
The supplementary search report has been based on the last set of claims valid and available at the start of the search.			
Place of search		Date of completion of the search	Examiner
Munich		28 September 2004	Rolan Cisneros, E
CATEGORY OF CITED DOCUMENTS X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons &: member of the same patent family, corresponding document			

 2
 EP 02 70 4344 (P.05/06)

BEST AVAILABLE COPY

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 02 70 4344

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

28-09-2004

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
US 5383208	A	17-01-1995	FR	2694423 A1	04-02-1994
			DE	69304844 D1	24-10-1996
			DE	69304844 T2	30-01-1997
			EP	0583186 A1	16-02-1994
			JP	6097548 A	08-04-1994
US 5953690	A	14-09-1999	AU	3500697 A	21-01-1998
			WO	9800943 A1	08-01-1998
US 5812572	A	22-09-1998	AU	3508797 A	21-01-1998
			WO	9800893 A1	08-01-1998
US 5019769	A	28-05-1991	AU	654825 B2	24-11-1994
			AU	8448391 A	15-04-1992
			DE	69127700 D1	23-10-1997
			DE	69127700 T2	19-03-1998
			EP	0548111 A1	30-06-1993
			JP	3248720 B2	21-01-2002
			JP	6504405 T	19-05-1994
			WO	9205608 A1	02-04-1992
US 5396059	A	07-03-1995	US	5278404 A	11-01-1994
			EP	0580317 A1	26-01-1994
			JP	6209290 A	26-07-1994
US 5594748	A	14-01-1997	AU	6722996 A	05-03-1997
			WO	9706586 A1	20-02-1997

BEST AVAILABLE COPY

EP 02 70 4344

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

TOTAL P.06